

CLAIMS

Therefore, having thus described the invention, at least the following is claimed:

- 1 1. A method for fabricating micro-electro-mechanical system (MEMS) capacitive resonators, the method comprising:
 - 3 forming trenches in a substrate;
 - 4 conformally coating the substrate with an oxide;
 - 5 filling the coated trenches with polysilicon;
 - 6 patterning the polysilicon;
 - 7 releasing a resonator structure derived from the substrate; and
 - 8 removing the conformally coated oxide.
- 1 2. The method of claim 1, further comprising:
 - 2 depositing nitride on at least one of an insulating layer and the substrate;
 - 3 patterning the nitride to isolate pads;
 - 4 providing polysilicon to the patterned pads; and
 - 5 metallizing the pads.
- 1 3. The method of claim 1, wherein the releasing comprises separating the resonating structure from the polysilicon.
- 1 4. The method of claim 1, wherein the releasing comprises an isotropic silicon etching of the resonator.
- 1 5. The method of claim 1, wherein the filling includes filling out from sidewalls of the trenches.
- 1 6. The method of claim 1, wherein the removing includes forming a gap between the resonator structure and the polysilicon in a self-aligned manner.

- 1 7. The method of claim 6, wherein the gap is approximately less than 90 nanometers.
- 1 8. The method of claim 1, wherein the filling includes forming an electrode.
- 1 9. The method of claim 1, wherein the etching includes forming high-aspect ratio
2 trenches.
- 1 10. A micro-electro-mechanical system (MEMS) capacitive resonator, comprising:
2 a semiconductor resonating member; and
3 a polysilicon electrode comprised of a different material than the semiconductor
4 resonating member, wherein the polysilicon electrode is capacitively coupled to the
5 semiconductor resonating member.
- 1 11. The resonator of claim 10, wherein the polysilicon electrode is capacitively
2 coupled to the semiconductor resonating member over a gap ranging from one of
3 approximately 700 – 1000 nanometers (nm), 90 – 700 nm, and less than 90 nm.
- 1 12. The resonator of claim 10, wherein the semiconductor resonating member has a
2 width ranging from approximately 5.5 – 7.5 microns, a length for the corresponding
3 width ranging from approximately 300 – 1100 microns; a first flexural mode frequency
4 response for the corresponding width and length ranging from approximately 40 kilohertz
5 – 528 kilohertz, and a quality factor for the first flexural frequency response ranging from
6 approximately 17,000 – 67,000.
- 1 13. The resonator of claim 10, wherein the semiconductor resonating member has a
2 width of approximately 5.5 – 6.5 microns, a length for the corresponding width ranging
3 from approximately 300 – 1100 microns, a first flexural mode frequency response for the
4 corresponding width and length ranging from approximately 40 kilohertz – 528 kilohertz,
5 and a quality factor for the first flexural frequency response ranging from approximately
6 17,000 – 67,000.

- 1 14. The resonator of claim 10, wherein the semiconductor resonating member
- 2 includes one of a beam and a block.
- 1 15. The resonator of claim 10, wherein the semiconductor resonating member has a
- 2 thickness ranging from one of 5 microns to 40 microns, 10 to 40 microns, 20 to 40
- 3 microns and 30-40 microns.
- 1 16. The resonator of claim 10, wherein the resonator is a MEMS device.
- 1 17. The resonator of claim 10, wherein a gap inherent to the capacitive coupling is
- 2 formed in a self-aligned manner using a sacrificial layer in between the semiconductor
- 3 resonating member and the polysilicon electrode.
- 1 18. A method for fabricating micro-electro-mechanical system (MEMS) capacitive
- 2 resonators, the method comprising:
 - 3 forming trenches in a semiconductor-on-insulator substrate;
 - 4 conformally coating the semiconductor-on-insulator substrate with an oxide;
 - 5 filling the coated trenches with polysilicon, wherein electrodes are derived from
 - 6 the polysilicon;
 - 7 forming release openings; and
 - 8 removing the conformally coated oxide and an oxide of the semiconductor-on-
 - 9 insulator substrate, wherein a capacitive gap is formed, wherein a resonating element of
 - 10 the capacitive resonator is released.

1 19. The method of claim 18, further including:
2 growing and patterning an insulator oxide, wherein the insulator oxide provides
3 isolation between the semiconductor-on-insulator substrate and wire-bonding pads;
4 depositing and patterning nitride, wherein the nitride provides protection for the
5 insulator oxide disposed on the pads;
6 growing and removing a surface treatment oxide, wherein the surface treatment
7 oxide enables the reduction of the roughness of sidewalls of the resonating element;
8 depositing polysilicon to form the wirebonding pads for drive and sense
9 electrodes;
10 metallizing the pads; and
11 patterning the polysilicon inside the trenches.

1 20. The method of claim 18, wherein the forming release openings comprises
2 anisotropically etching to an oxide layer of the semiconductor-on-substrate, such that the
3 undercut of the resonating element is facilitated.

1 21. The method of claim 18, wherein the filling includes one of filling the trenches
2 with doped LPCVD polysilicon such that the electrodes are formed vertically and
3 depositing and patterning doped LPCVD polysilicon.

1 22. The method of claim 18, wherein the forming trenches includes one of deep
2 reactive ion etching and regular reactive ion etching to an oxide layer of the
3 semiconductor-on-insulator substrate.

1 23. The method of claim 18, wherein the conformally coating includes depositing a
2 LPCVD high-temperature oxide of approximately less than 100 nanometers.

1 24. The method of claim 18, wherein the conformally coating is scalable to
2 correspond to a desired thickness of a lateral gap spacing for the capacitive resonator.

1 25. The method of claim 18, wherein the removing comprises an anisotropic plasma
2 etching such that at least a portion of the oxide remains on sidewalls of the resonating
3 element.

1 26. The method of claim 18, wherein the releasing comprises exposing the
2 semiconductor-on-insulator substrate to a solution comprising HF:H2O to release the
3 resonating element from a handle layer and the electrodes.

1 27. The method of claim 18, wherein the forming trenches includes etching high-
2 aspect ratio trenches.

1 28. The method of claim 18, wherein the removing includes forming a gap between
2 the resonating element and the polysilicon in a self-aligned manner.

1 29. A semiconductor-on-insulator (SOI) micro-electro-mechanical system (MEMS)
2 capacitive resonator, comprising:
3 a semiconductor resonating member; and
4 a polysilicon electrode comprised of a different material than the semiconductor
5 resonating member, wherein the polysilicon electrode is capacitively coupled to the
6 semiconductor resonating member.

1 30. The resonator of claim 29, wherein the polysilicon electrode is capacitively
2 coupled to the semiconductor resonating member over a gap of approximately 90
3 nanometers.

1 31. The resonator of claim 29, wherein the semiconductor resonating member has at
2 least one of a flexural and bulk-mode frequency response ranging from approximately 3
3 MHz – 300 MHz and a quality factor over at least one of approximately 10,000, 20,000,
4 and 30,000.

- 1 32. The resonator of claim 29, wherein the semiconductor resonating member
- 2 includes one of a disk, a beam, and a block.

- 1 33. The resonator of claim 32, wherein the disk is supported on its side at one of a
2 location corresponding to a resonating node and a plurality of resonating nodes.

- 1 34. The resonator of claim 29, wherein the semiconductor resonating member has a
2 thickness ranging from one of 5 microns to 40 microns, 10 to 40 microns, 20 to 40
3 microns and 30-40 microns.

- 1 35. The resonator of claim 29, wherein a gap inherent to the capacitive coupling is
2 formed in a self-aligned manner using a sacrificial layer in between the semiconductor
3 resonating member and the polysilicon electrode.